This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-77 (Cancelled).

78. (Original) A method of forming a photosensor of a pixel cell, said method comprising:

forming a first doped layer of a first conductivity type in said substrate;

forming a doped region of a second conductivity type in said first doped layer and between a gate structure and an isolation region; and

forming an implanted region of said first conductivity type in said substrate, said implanted region being lateral of and in contact with said doped region.

79. (Original) The method of claim 78, wherein said implanted region is formed along at least a portion of the bottom of said gate structure.

80. (Original) The method of claim 78, wherein said implanted region is formed by implanting a p-type dopant below at least a portion of said gate structure.

81. (Original) The method of claim 78, wherein said implanted region is doped with a p-type dopant at a dopant concentration of about 1 x 10^{16} to about 1 x 10^{17} atoms per cm^3.

82. (Original) The method of claim 81, wherein said implanted region is doped with a p-type dopant at a dopant concentration of about 5 x10^{15} to about 5 x10^{16} atoms per cm^3.

83. (Original) The method of claim 78, wherein said implanted region is formed to a thickness of about 0.5 microns to about 7.0 microns.

84. (Original) The method of claim 83, wherein said implanted region is formed to a thickness of about 1.0 microns to about 5.0 microns.

85. (Original) The method of claim 78, wherein said act of forming said implanted region further comprises forming a photoresist layer over said gate structure and said substrate, and patterning and etching said photoresist layer to expose an area of said substrate located between said isolation region and said doped region.

86. (Original) The method of claim 85 further comprising the act of implanting a p-type dopant below said area of said substrate.

87. (Original) The method of claim 86 further comprising forming a second doped layer of said first conductivity type in said substrate and above said doped region.

88. (Original) The method of claim 78, wherein said photosensor is a photodiode.

89. (Original) The method of claim 88, wherein said photodiode is an n-p photodiode.

90. (Original) The method of claim 88, wherein said photodiode is a p-n photodiode.

91. (Original) The method of claim 88, wherein said photodiode is a p-n-p photodiode.

92. (Original) The method of claim 88, wherein said photodiode is an n-p-n photodiode.

93. (Original) The method of claim 78, wherein said photosensor is a photogate.

94. (Original) The method of claim 78, wherein said photosensor is a photoconductor.

95. (Original) The method of claim 78, wherein said gate structure is a transfer gate.

96. (Original) The method of claim 78, wherein said gate structure is a reset gate.

97. (Original) A method of forming a photosensor for an imaging device, said method comprising:

forming a gate of a transistor over a silicon substrate;

forming a first p-type doped layer in said silicon substrate;

forming an n-type doped region below said first p-type doped layer; and

forming a doped region lateral of and in contact with said n-type doped region by implanting p-type ions below at least a portion of said gate and within an implant area of said silicon substrate, said doped region having a dopant concentration within the range of from about 1×10^{16} to about 1×10^{17} atoms per cm^3.

98. (Original) The method of claim 97, wherein said doped region is formed along at least a portion of the bottom of said gate.

99. (Original) The method of claim 97, wherein said gate is a transfer gate of a transfer transistor.

100. (Original) The method of claim 97, wherein said gate is a reset gate of a reset transistor.

101. (Original) The method of claim 97, wherein said doped region is formed to a thickness of about 0.5 microns to about 7.0 microns.

102. (Original) The method of claim 101, wherein said doped region is formed to a thickness of about 1.0 microns to about 5.0 microns.

103. (Original) The method of claim 97, wherein said act of forming said doped region further comprises forming a photoresist layer over said gate and said substrate, and patterning and etching said photoresist layer to expose said implant area of said substrate.

104. (Original) The method of claim 103 further comprising the act of forming said implant area between said isolation region and said n-type doped region.

105. (Original) The method of claim 104 further comprising the act of implanting a p-type dopant below said implant area of said substrate.

106. (Original) A method of forming a barrier implanted region within a channel region of a transistor, said method comprising:

forming a gate structure of a transistor over a substrate;

forming source and drain regions of a first conductivity type on opposite sides of said gate structure, said source and drain regions forming a channel region within said substrate and between said source and drain regions; and

forming a barrier implanted region of a second conductivity type within said channel region and adjacent said gate structure, said barrier implanted region having a barrier dopant concentration higher than the substrate dopant concentration.

107. (Original) The method of claim 106, wherein said barrier implanted region is formed by implanting ions below at least a portion of said gate and within said substrate.

108. (Original) The method of claim 106, wherein said barrier implanted region has a dopant concentration within the range of from about 1 x 10^{16} to about 1 x 10^{17} atoms per cm^3.

109. (Original) The method of claim 108, wherein said barrier implanted region has a dopant concentration of about 5 x10^{15} to about 5 x10^{16} atoms per cm^3.

110. (Original) The method of claim 106, further comprising the step of forming a charge collection region of said first conductivity type lateral of and adjacent said barrier implanted region.

111. (Original) The method of claim 106, wherein said gate structure is a transfer gate.

112. (Original) The method of claim 106, wherein said gate structure is a reset gate.